SGS **MOS INTEGRATED CIRCUIT**

M 109

PRELIMINARY DATA

DIGITAL ACCOMPANIMENT INTERFACE

- 8-BIT BIDIRECTIONAL BUS (6 AS DATA AND 2 AS STROBE) FOR EASY INTERFACE WITH ANY MICROPROCESSOR
- STANDARD SOFTWARE AVAILABLE FOR F8 MONOCHIP MICROPROCESSOR FAMILY (3870, 3872, etc.)
- 5 KEYS ACCEPTED (CHANNEL A, B, C, D, E) IN A RANGE OF 3 OCTAVES (36 KEYS)
- SEPARATED OUTPUTS (WITH MORE FOOTAGES) FOR EACH KEY ACCEPTED: 9 FOR THE KEYS A, B AND C (8' 12.5% DUTY CYCLE, 4' AND 2' 50% DUTY CYCLE) AND 4 FOR THE KEYS D AND E (8' 12.5% DUTY CYCLE AND 4' 50% DUTY CYCLE)
- 3 OUTPUTS, USABLE AS ARPEGGIO, SWITCHING THE CONTENTS OF THE KEYS A, B AND C IN 4 OCTAVES
- BASS OUTPUTS, INDEPENDENT OF THE FIVE KEYS, WITH FIVE FOOTAGES OCTAVE RELATED
- 6 TRIGGER SIGNALS AVAILABLE: "TP", "TS" AND "TP-EX-OR TS" FOR BASS, "TDA" FOR ARPEGGIO, "NP" AND "KP" FOR KEYBOARD WITH OR WITHOUT MEMORIZATION
- INTERNAL TOP OCTAVE SYNTHESIZER WITH CHOICE BETWEEN 2 OR 1 MHz INPUT CLOCK
- OPEN DRAIN OUTPUTS FOR ALL THE FREQUENCIES AND TRIGGERS
- STANDARD SINGLE SUPPLY: +5V ± 5%
- LOW DISSIPATION: ⩽ 500 mW
- INPUTS PROTECTED FROM ELECTROSTATIC DISCHARGES

The M109 is realized on a single monolithic silicon chip, using N-channel silicon gate technology.
It is available in a 40 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS

V_o	Voltage (at open drain pins)	-0.3 to +13.5	V
V_i	Voltage at any pin with respect to ground (except open drain pins)	-0.3 to +7	V
I_o	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 50	°C

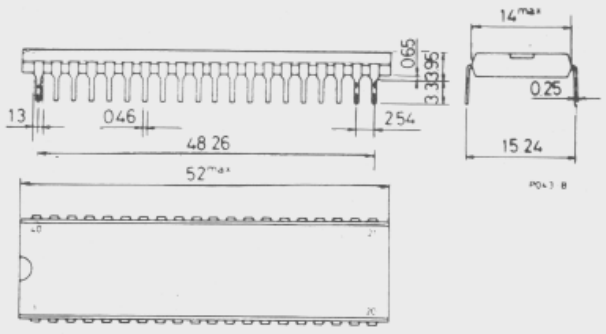
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBER: M109 B1 for dual in-line plastic package

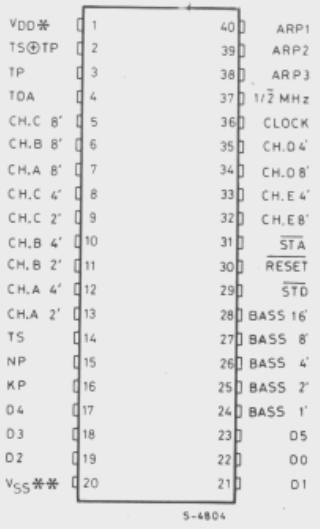
M 109

MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package

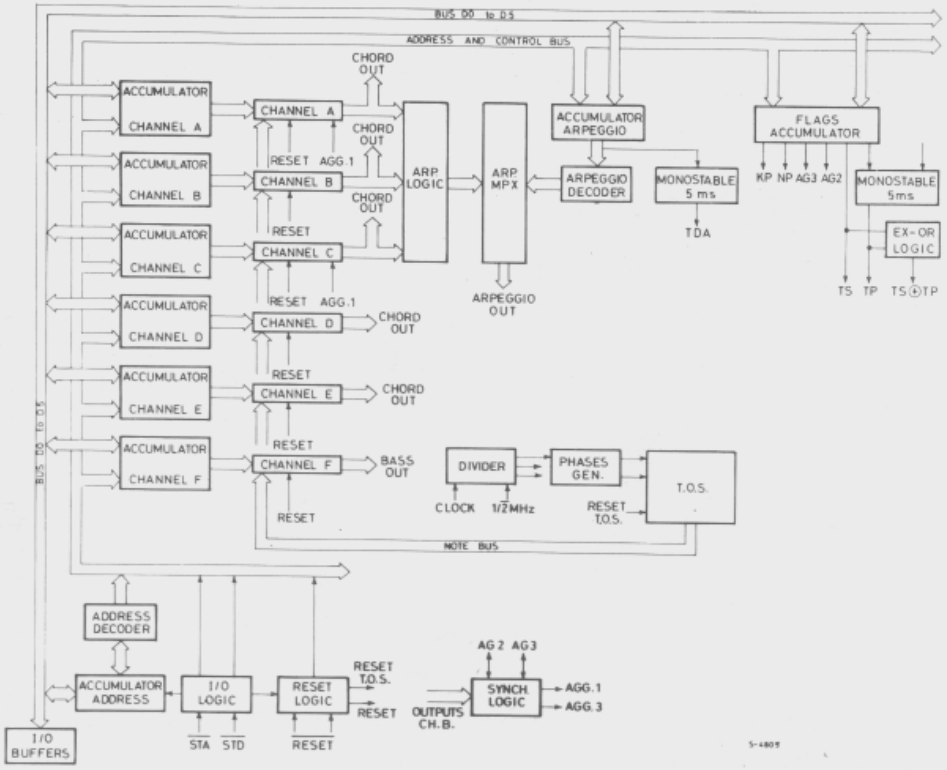


PIN CONNECTIONS



* V_{DD} is the highest supply voltage
** V_{SS} is the lowest supply voltage

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		4.75	5	5.25	V

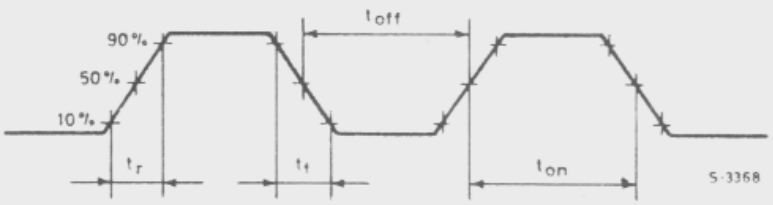
STATIC ELECTRICAL CHARACTERISTICS (V_{DD} = +5V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 50°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
INPUT SIGNALS						
Clock	V_{IL}		0	0	0.6	V
	V_{IH}		2.2	5	6	V
D0 to D5	V_{IL}		0	0	0.6	V
	V_{IH}		2.2	5	6	V
	R_{ON}	V_{OH} = 1V			500	Ω
$\overline{DA}$, $\overline{STD}$	V_{IL}		0	0	0.6	V
	V_{IH}		2.2	5	6	V
1/$\overline{2}$ MHz	V_{IL}		0	0	0.6	V
	V_{IH}		2.2	5	6	V
$\overline{RESET}$	V_{IL}		0	0	0.6	V
	V_{IH}		2.2	5	6	V
OUTPUT SIGNALS (all open drain)						
V_{OL}		I_{OL} = 1 mA			1	V
I_{LO}		V_{OH} = +12V			10	μA

DYNAMIC ELECTRICAL CHARACTERISTICS

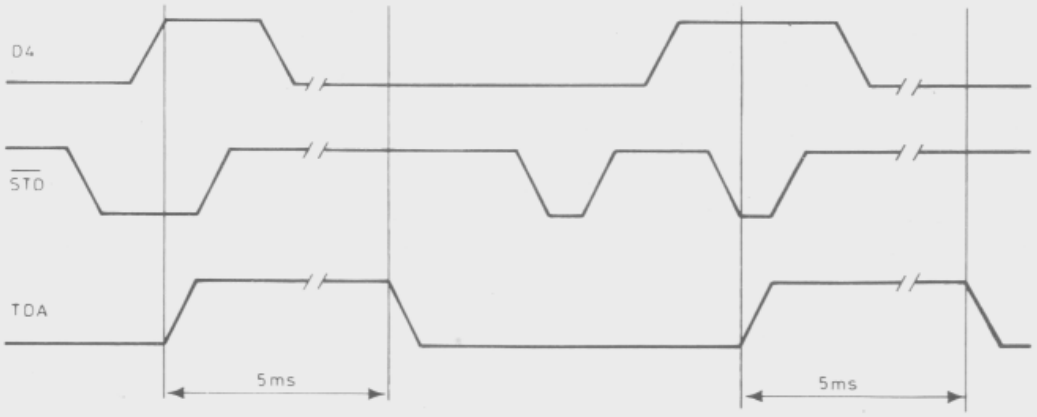
Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK						
f_i	Input clock frequency	1/2 MHz Input = +5V	100	1000.12	1500	KHz
t_r, t_f	Input clock rise and fall times 10% to 90%				30	ns
$\overline{STA}$, $\overline{STD}$						
t_W	Pulse width	At 50% of duty cycle	4			µs
TDA, TP OUTPUTS						
t_{on}	Pulse duration	At 50% of duty cycle	4.5		5.5	ms
$\overline{RESET}$						
t_r	Rise time				30	ns

INPUT CLOCK WAVEFORM



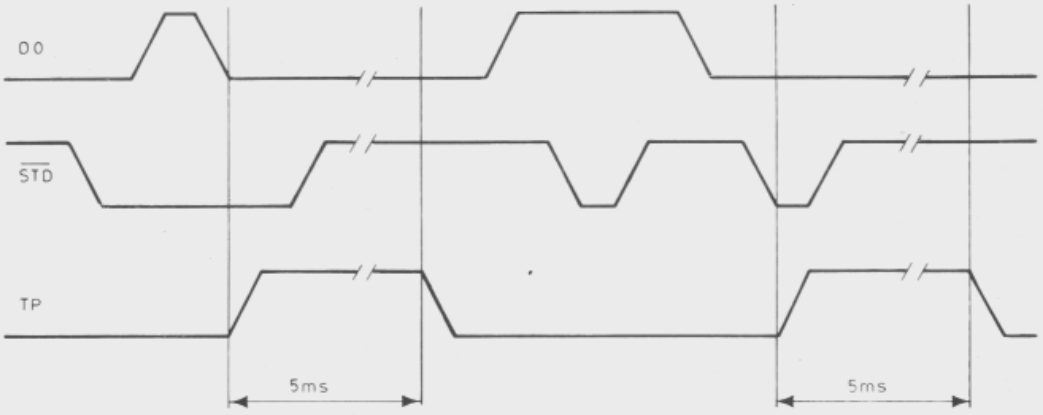
TIMING DIAGRAMS

"TDA"



TIMING DIAGRAMS (continued)

"TP"



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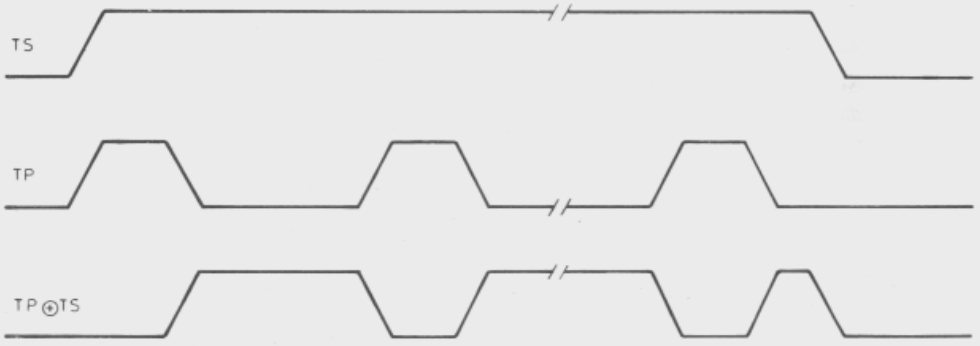
"TP ⊕ TS"



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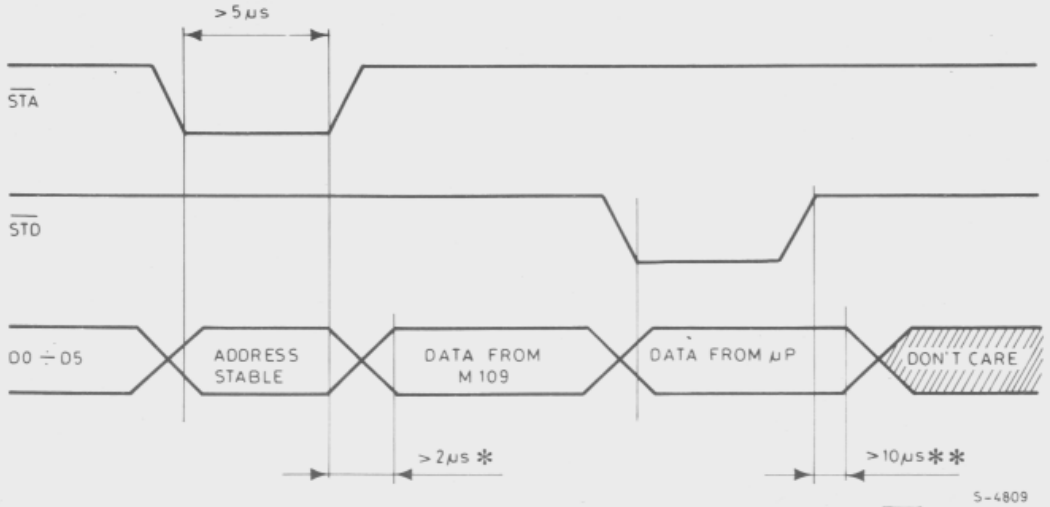
ACCUMULATOR LOADING



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* The data from the M109 can be read after a time > 2 μs from the positive going edge of $\overline{STA}$.

** The data from the microprocessor must be maintained for a time > 10 μs after the positive going edge of $\overline{STD}$.

GENERAL CHARACTERISTICS

The M109 (Digital Accompaniment Interface) is a device for musical applications (electronic organs, etc.) which, connected with a microprocessor, generates the outputs of chords, arpeggio, bass and triggers. It consists basically of a T.O.S. (Top Octave Synthesizer), dividers, 8 accumulators connected by a di-directional bus to the microprocessor, 5 sound channel for the chords, 1 for the bass and 3 MPX for the arpeggio (see block diagram).
The circuit comprises:

a) 2 pins for clock input and clock frequency control; the control allows the bypass of the divider in the input of the T.O.S.: when the control is to GND the divider is connected between the clock input and the T.O.S.
When the control is to V_{DD} the divider is bypassed; in both cases (clock of 2000.24 or 1000.12 KHz) the T.O.S. can receive the correct clock of 1000.12 KHz.

b) 8 pins as bidirectional bus from the microprocessor: 6 are used as data (D0 to D5) and 2 as strobe ($\overline{STA}$ = Strobe Address, $\overline{STD}$ = Strobe Data), the two strobes are active low.

c) 13 chord outputs for the five keys accepted.
Channels A, B, C have 3 outputs each: 8' 12.5% of duty cycle, 4' and 2' 50%; channels D and E have only 2 outputs each: 8' 12.5% and 4' 50%.
The 5 channels can play in a range of 3 octaves, from C (Do) to B (Si) and the range of frequencies is: 65.4 Hz (C) to 493.8 Hz (B) for 8'; 130.8 to 987.7 Hz for 4'; 261.6 to 1975.5 Hz for 2'.
All these outputs are open drain.

d) 3 outputs for arpeggio: these outputs depend on the channels A, B and C. In fact, according to the codes coming from the microprocessor, they can select from among them the notes of the 3 channels in a range of further 4 octaves.
All these outputs are open drain.

e) 5 outputs for bass: each output gives the same note but in 5 different footages: 16', 8', 4', 2', 1' 50% duty cycle. These outputs are also open drain.

f) 6 trigger outputs: "TDA" (Trigger Decay Arpeggio) is a pulse which can appear when a new arpeggio code is coming, "KP" (Key Pressed) and "NP" (Note Present) are DC levels concerning the keyboard status: the exact configuration can be changed by software.
Usually "KP" is active only if there are keys pressed and "NP" is active when the notes are memorized in the outputs.
"TP" (Pulse) and "TS" (DC level) can be used as bass triggers: the first one for the percussion and the second one for the sustain.
In the end there is "TP EX-OR TS" which is the logical EX-OR of TP and TS.
These outputs are also all open drain.

g) 1 input for Reset (low active) which provides the reset of the T.O.S., the dividers, the registers and all the parts of the device.

h) 2 supply pins.

ACCUMULATOR AND INPUT-OUTPUT LOGIC

The M109 includes eight accumulators, readable and alterable by the microprocessor. Six of the eight bits of the microprocessor are connected to the bidirectional bus of the microprocessor and used as data; two are used as strobe address ($\overline{STA}$) and strobe data ($\overline{STD}$).
The address code of the accumulator (3 bits) is loaded before the data on bits D0 to D2 of the bus and is transferred to the addressed accumulator by an internal strobe generated by the negative-going transition of $\overline{STA}$, while the data is loaded on the accumulators addressed on the negative-going tran-

sition of $\overline{STD}$ and memorized on the positive-going transition of $\overline{STD}$ (see timing diagram accumulator loading). The functions of the 8 accumulators are as follows:

Accumulator channel A: drives chord channel "A" and consists of 6 bits: the note code (bits D0 to D3) and the octave code (bits D4 to D5).

Accumulator channel B: same for chord channel "B".

Accumulator channel C: same for chord channel "C".

Accumulator channel D: same for chord channel "D".

Accumulator channel E: same for chord channel "E".

Accumulator F (Bass): drives the bass channel with the same code meaning of the chord channels.

Accumulator G (Flags): drives 6 flag signals and consists of 6 bits (see flag chapter).

Accumulator H (Arpeggio): consists of 5 bits and includes the arpeggio codes (bits D0 to D3) and the valid arpeggio code (D4) necessary for the trigger "TDA" (see table 6).

TABLE 1 — Accumulator Addresses

D2	D1	D0	Accumulators
0	0	0	Channel A
0	0	1	Channel B
0	1	0	Channel C
0	1	1	Channel D
1	0	0	Channel E
1	0	1	Channel F (Bass)
1	1	0	Channel G (Flags)
1	1	1	Channel H (Arpeggio MPX)

CHORD CHANNELS

Channel A : consists of a note decoder which has the 4 bits of notes D0 to D3 of the accumulator "A" in input and selects one of the 12 notes generated by the T.O.S. or GND (no note played); the selected note enters a chain of five dividers; the first two can be bypassed by a strobe generated by the octave logic, which receives the two octave bits, D4 to D5, from accumulator "A". All divider outputs are sent to the arpeggio logic, while only some are sent to the outputs.
Table 2 shows the note codes, and table 3 shows the octave codes.

Channel B : has the same structure as channel A, but with a further divider at the end of the chain; it receives the octave and note codes from accumulator "B".

Channel C : has the same configuration as channel B and receives the codes from accumulator "C".

Channel D : has the same configuration as channel A (5 dividers) and receives the codes from accumulator "D". The divider outputs are connected to the outputs only.

Channel E : identical to channel D and receives the codes from accumulator "E".

Synchronisation logic: it is possible to load the same note on channels A, B and C (so that there is always a note in the arpeggio outputs): in this case phase problems must be avoided. The synchronisation logic, controlled by the microprocessor, synchronizes channels A and C to channel B by 2 bits D3 of the flag accumulator.
This logic consists of a monostable which generates a reset pulse for the channels to synchonize when all the right outputs of channels B go to zero. In this case only channel B is playing and the outputs of channels A and C are disenabled.

TABLE 2 — Note Codes

D3	D2	D1	D0	Note
0	0	0	0	GND
0	0	0	1	C (DO)
0	0	1	0	C # (DO #)
0	0	1	1	D (RE)
0	1	0	0	D # (RE #)
0	1	0	1	E (MI)
0	1	1	0	F (FA)
0	1	1	1	F # (FA #)
1	0	0	0	G (SOL)
1	0	0	1	G # (SOL #)
1	0	1	0	A (LA)
1	0	1	1	A # (LA #)
1	1	0	0	B (SI)

TABLE 3 — Octave Codes

D5	D4	1st divider	2nd divider
0	0	dividing	dividing
0	1	dividing	dividing
1	0	not dividing	dividing
1	1	not dividing	not dividing

BASS CHANNEL

This consists of a note decoder, a note multiplexer and a chain of 7 dividers; the first 3 dividers can be bypassed by strobes generated by the octave logic.
It receives the code from accumulator "F". The meaning of the note codes is the same as the chord channels; the octave codes are shown in table 4.

The dividers of the bass channel change on the negative-going edge, whereas the dividers of channels "A" to "E" change on the positive-going edge.

TABLE 4 – Bass Octave Codes

D5	D4	1st divider	2nd divider	3rd divider
0	0	dividing	dividing	dividing
0	1	dividing	dividing	not dividing
1	0	dividing	not dividing	not dividing
1	1	not dividing	not dividing	not dividing

ARPEGGIO MULTIPLEXER

This multiplexer consists of 3 MPX which receive from the inputs the frequencies generated by the dividers of channels "A", B and C", followed by a logic circuit to select the duty cycle (12.5, 25 or 50%); the outputs are connected to the arpeggio outputs (ARP 1, 2, 3), see table 6.
The selection of the input line is dependent on the arpeggio codes (accumulator "G" bits D0 to D3); bit D4 can be used to drive a monostable which gives the TDA pulse (Trigger Decay Arpeggio) of 5 ms when a new valid code is sent to the accumulator (see timing diagram of "TDA").

FLAGS

Accumulator "G", connected to the bidirectional bus, can be written or read like the other; it contains 6 bits of flag some of which are sent directly to the outputs and some are used to generate triggers. (see table 5).

TABLE 5

All the flag signals are active high.

D0	This bit is used to generate pulse "TP" (see timing diagram of TP).
D1	This generates "TS" (DC level) directly.
D2	This is used for the synchronism logic, it denotes: "channel A, B and C with the same note (only one key pressed)".
D3	It is used for the synchronism logic, it denotes: "channels B and C with the same note (two keys pressed)".
D4	It generates "NP" (DC level) directly.
D5	It generates "KP" (DC level) directly.

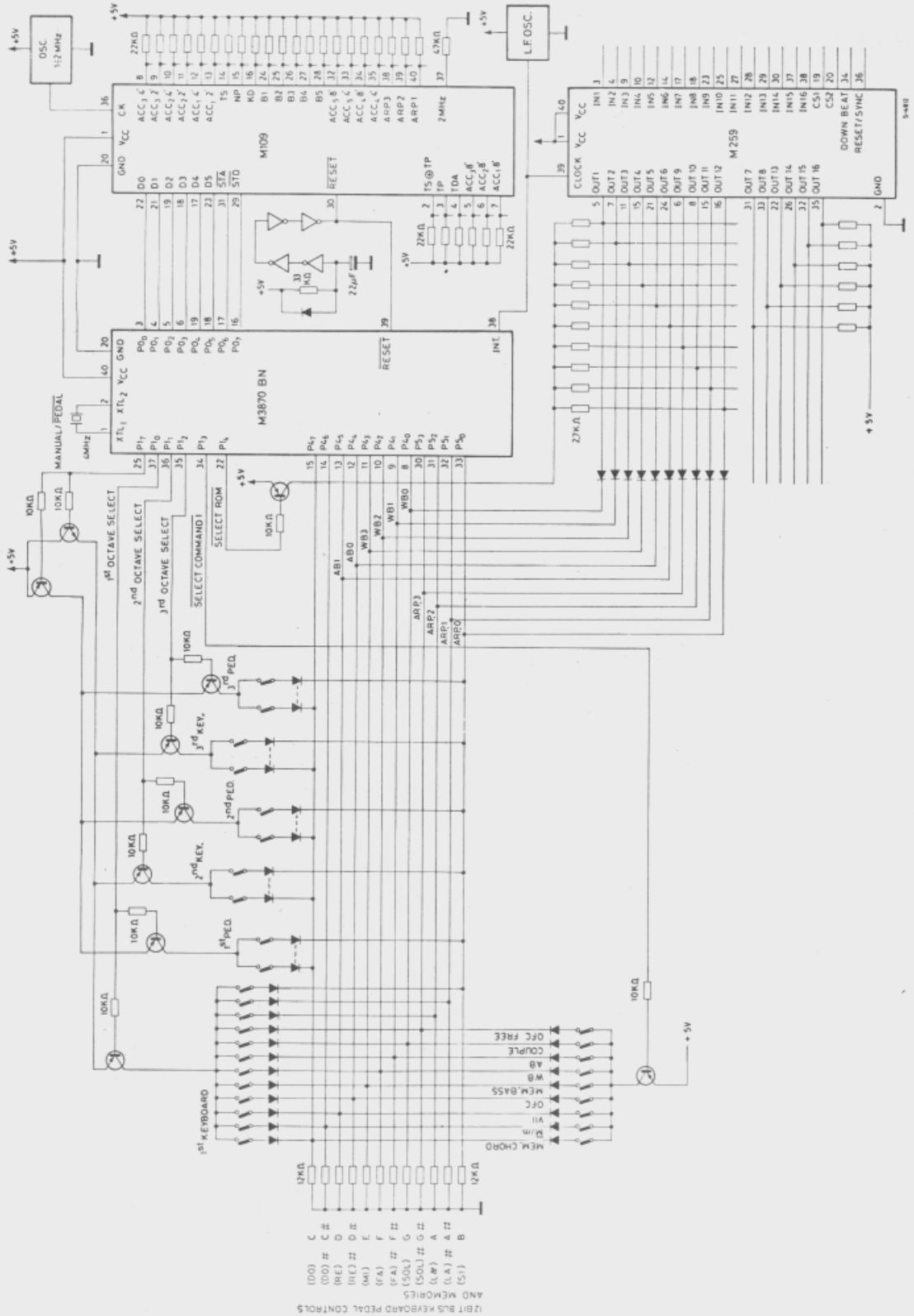
Signals "TP" and "TS" are also combined in a logic network to give at the output the logical EX-OR of the signals (see timing diagram of "TP ⊕ TS").

TABLE 6 – Arpeggio Codes

CODE				ARP 1				ARP 2				ARP 3			
3	2	1	0	Accomp. channel	Foot	Octave from	to	Duty cycle	Accomp. channel	Foot	Octave from	to	Duty cycle	Accomp. channel	Foot	Octave from	to	Duty cycle
0	0	0	1	CH B	8′	C1	B3	12.5	CH A	8′	C1	B3	12.5	CH C	16′	C0	B2	12.5
0	0	1	0	CH A	8′	C1	B3	12.5	CH C	16′	C0	B2	12.5	CH B	16′	C0	B2	12.5
0	0	1	1	CH C	8′	C1	B3	12.5	CH B	8′	C1	B3	12.5	CH A	8′	C1	B3	12.5
0	1	0	0	CH B	2′	C3	B5	*	CH A	2′	C3	B5	*	CH C	4′	C2	B4	12.5
0	1	0	1	CH A	2′	C3	B5	*	CH C	4′	C2	B4	12.5	CH B	4′	C2	B4	12.5
0	1	1	0	CH C	2′	C3	B5	*	CH B	2′	C3	B5	*	CH A	2′	C3	B5	*
0	1	1	1	CH B	4′	C2	B4	12.5	CH A	4′	C2	B4	12.5	CH C	8′	C1	B3	12.5
1	0	0	0	CH A	4′	C2	B4	12.5	CH C	8′	C1	B3	12.5	CH B	8′	C1	B3	12.5
1	0	0	1	CH C	4′	C2	B4	12.5	CH B	4′	C2	B4	12.5	CH A	4′	C2	B4	12.5
1	0	1	0	CH B	1′	C4	B6	*	CH A	1′	C4	B6	*	CH C	2′	C3	B5	*
1	0	1	1	CH A	1′	C4	B6	*	CH C	2′	C3	B5	*	CH B	2′	C3	B5	*
1	1	0	0	CH C	1′	C4	B6	*	CH B	1′	C4	B6	*	CH A	1′	C4	B6	*
				N.C.					N.C.					N.C.				

* C1 is the C of the first octave to the left and B3 is the B of the third octave to the left; the notes from C0 to B4 have a 12.5% duty cycle, from B4 to B5 with 25% duty cycles and from B5 to B6 with 50% duty cycle.

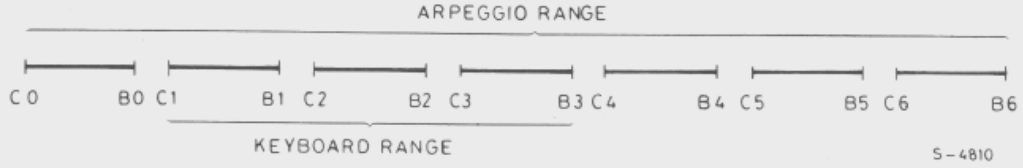
TYPICAL APPLICATION



RANGE OF FREQUENCIES

Keyboard: for C1 (1st key on the left of the keyboard)
Arpeggio: C0 = 32.7 Hz, B6 = 3951 Hz

8′ = 65.4 Hz (12.5% duty cycle)
4′ = 130.8 Hz (50% duty cycle)
2′ = 261.6 Hz (50% duty cycle)



Pedal board: for CA (1st key on the left)

16′ = 16.3 Hz
8′ = 32.7 Hz
4′ = 65.4 Hz
2′ = 130.8 Hz
1′ = 261.6 Hz